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09/934,601	08/23/2001	Takao Inoue	500.40552X00	8550

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EXAMINER	
GANDHI, DIPAKKUMAR B	

ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/934,601	INOUE ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-16 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 23 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 3, 8/23/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikeda et al. (US 2003/0023909 A1).

Ikeda et al. anticipate claim 1.

Ikeda et al. teach a turbo decoder (figure 12, page 5, paragraph 120, Ikeda et al.) comprising: a first and a second error correction decoder for error-correction decoding encoded data (coder 41 and coder 43 in figure 11, soft output decoder 51 and soft output decoder 53 in figure 12, page 10, paragraphs 258 and 259, Ikeda et al.); an interleaver memory for storing a soft output decoded result calculated by said first decoder as an interleaver input sequence (figure 7, 9, page 7, paragraph 221, Ikeda et al.); and an interleave address generator for generating write addresses for storing said interleaver input sequence in said interleaver memory, and read addresses for randomly reading an interleaver input sequence stored in said interleaver memory (figure 7, page 5, paragraph 115, Ikeda et al.), wherein said interleave address generator adds an offset to a symbol number for said interleaver input sequence for correction, and converts the corrected symbol number for said interleaver input sequence to generate the read address (figure 7, 10, page 8, paragraph 223, 229, 231, Ikeda et al.) when an address for randomly reading the

interleaver input sequence stored in said interleaver memory exceeds the number of bits resulting from a subtraction of tail bits from the number of information bits of the interleaver input sequence (figure 7, page 8, paragraph 230-235, Ikeda et al.).

- Ikeda et al. anticipate claim 2.

Ikeda et al. teach that the interleave address generator specifies the symbol numbers for the interleaver input sequence as addresses at which the interleaver input sequence is stored in said interleaver memory (figure 7, 9, page 7, paragraph 221, page 8, paragraph 230, Ikeda et al.) and sequentially converts the symbol numbers for the interleaver input sequence stored in said interleaver memory to generate the read addresses for the interleaver input sequence stored in said interleaver memory (page 8, paragraph 232, Ikeda et al.) .

- Ikeda et al. anticipate claim 3.

Ikeda et al. teach a turbo decoder, wherein said interleave address generator comprises: an output symbol number generator for sequentially generating symbol numbers for an interleaver input sequence stored in the interleaver memory (figure 7, page 8, paragraph 230, Ikeda et al.); and a threshold selector for setting a unique threshold for each of the symbol numbers generated by said output symbol number generator (page 6, paragraph 166, page 8, paragraph 229, 231, Ikeda et al.).

- Ikeda et al. anticipate claim 4.

Ikeda et al. teach a turbo decoder wherein the threshold selector selects a plurality of thresholds in accordance with the number of information bits of said interleaver input sequence, wherein said thresholds each correspond to an output symbol number generated by said output symbol number generator for each of the number of information bits of said interleaver input sequence, said output symbol number generator possibly generating an address, the value of which exceeds the number of bits excluding tail bits from the number of information bits of said interleaver input sequence (table 2, page 3, paragraph 69-74, page 6, paragraph 166, Ikeda et al.).

- Ikeda et al. anticipate claim 5.

Ikeda et al. teach a turbo decoder wherein the interleave address generator comprises an offset selector for selecting an offset, said offset being added to the output symbol number from said output symbol

number generator, in accordance with a threshold value selected from said threshold selector (page 6, paragraph 166, page 8, paragraph 229, 231, Ikeda et al.).

- Ikeda et al. anticipate claim 6.

Ikeda et al. teach a radio base station having an antenna, a radio frequency unit, a baseband unit, and a communication interface for interfacing said baseband unit with a communication network (figure 13, page 10, paragraph 267-268, page 11, paragraph 275, Ikeda et al.), wherein: said baseband unit comprises a turbo decoder for decoding encoded data (figure 12, page 5, paragraph 120, Ikeda et al.), said turbo decoder including: a first and a second error correction decoder for error-correction decoding encoded data (coder 41 and coder 43 in figure 11, soft output decoder 51 and soft output decoder 53 in figure 12, page 10, paragraphs 258 and 259, Ikeda et al.); an interleaver memory for storing soft output decoded results calculated by a plurality of said first decoders as an interleaver input sequence (figure 7, 9, page 7, paragraph 221, Ikeda et al.); and an interleave address generator for generating write addresses for storing said interleaver input sequence in said interleaver memory, and read addresses for randomly reading an interleaver input sequence stored in said interleaver memory (figure 7, page 5, paragraph 115, Ikeda et al.), wherein said interleave address generator adds an offset to a symbol number for said interleaver input sequence for correction, and converts the corrected symbol number for said interleaver input sequence to generate the read address (figure 7, 10, page 8, paragraph 223, 229, Ikeda et al.) when an address for randomly reading the interleaver input sequence stored in said interleaver memory exceeds the number of bits resulting from a subtraction of tail bits from the number of information bits of the interleaver input sequence (figure 7, page 8, paragraph 230-235, Ikeda et al.).

- Ikeda et al. anticipate claim 7.

Ikeda et al. teach a radio base station wherein: the interleave address generator specifies the symbol numbers for the interleaver input sequence as addresses at which the interleaver input sequence is stored in said interleaver memory (figure 7, 9, page 7, paragraph 221, page 8, paragraph 230, Ikeda et al.), and sequentially converts the symbol numbers for the interleaver input sequence stored in said interleaver memory to generate the read addresses for the interleaver input sequence stored in said interleaver memory (page 8, paragraph 232, Ikeda et al.) .

- Ikeda et al. anticipate claim 8.

Ikeda et al. teach a radio base station, wherein said interleave address generator comprises: an output symbol number generator for sequentially generating symbol numbers for an interleaver input sequence stored in said interleaver memory (figure 7, page 8, paragraph 230, Ikeda et al.); and a threshold selector for setting a unique threshold for each of the symbol numbers generated by said output symbol number generator (page 6, paragraph 166, page 8, paragraph 229, 231, Ikeda et al.).

- Ikeda et al. anticipate claim 9.

Ikeda et al. teach a radio base station wherein: the threshold selector selects a plurality of thresholds in accordance with the number of information bits of said interleaver input sequence, wherein said thresholds each correspond to an output symbol number generated by said output symbol number generator for each of the number of information bits of said interleaver input sequence, said output symbol number generator possibly generating an address, the value of which exceeds the number of bits excluding tail bits from the number of information bits of said interleaver input sequence (table 2, page 3, paragraph 69-74, page 6, paragraph 166, Ikeda et al.).

- Ikeda et al. anticipate claim 10.

Ikeda et al. teach a radio base station, wherein: said interleave address generator comprises an offset selector for selecting an offset, said offset being added to the output symbol number from said output symbol number generator, in accordance with a threshold value selected from said threshold selector (page 6, paragraph 166, page 8, paragraph 229, 231, Ikeda et al.).

- Ikeda et al. anticipate claim 11.

Ikeda et al. teach a turbo encoder comprising: a convolutional encoder for convolutional encoding transmission data (figure 11, page 9, paragraph 248-249, Ikeda et al.); an interleaver memory for storing transmission data (page 9, paragraph 251, Ikeda et al.); and interleave address generator (figure 7, page 8, paragraph 229, page 10, paragraph 252, Ikeda et al.); for generating write addresses for storing transmission data in said interleaver memory (page 7, paragraph 221, Ikeda et al.); and read addresses for randomly reading data comprising transmission data stored in said interleaver memory (figure 10, page 8, paragraph 223, Ikeda et al.); wherein said interleave address generator adds an offset to a

symbol number for each bit of the transmission data, and converts said corrected symbol number to generate the read address (figure 7, 10, page 8, paragraph 223, 229, 231, Ikeda et al.); when an address for randomly reading the transmission data stored in said interleaver memory exceeds the number of bits resulting from a subtraction of tail bits from the number of information bits of the transmission data (figure 7, page 8, paragraph 230-235, Ikeda et al.).

- Ikeda et al. anticipate claim 12.

Ikeda et al. teach a turbo encoder comprising: a plurality of convolutional encoders each for convolutional encoding information bits to be transmitted (figure 11, page 9, paragraph 248-249, Ikeda et al.); an interleaver memory for storing information bits to be transmitted (page 9, paragraph 251, Ikeda et al.); and an interleave address generator (figure 7, page 8, paragraph 229, page 10, paragraph 252, Ikeda et al.); for generating interleave addresses for randomly reading information bits stored in said interleaver memory (figure 10, page 8, paragraph 223, Ikeda et al.), wherein said interleave address generator converts a symbol number corresponding to an input symbol sequence to an address in accordance with a unique address conversion method to generate an interleave address, and corrects the symbol number in accordance with a previously determined rule and converts the corrected symbol number to generate the interleave address when the address converted from the symbol number does not match a previously set symbol number (figure 7, 10, page 8, paragraph 223, 229-235, Ikeda et al.).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda et al. (US 2003/0023909 A1) as applied to claim 12 above, and further in view of Pekarich et al. (US 6,549,998 B1).

As per claim 13, Ikeda et al. substantially teach the claimed invention described in claim 12 (as rejected above).

However Ikeda et al. do not explicitly teach the specific use of the interleave address generator comprising logic circuits.

Pekarich et al. in an analogous art teach a circuit for generating an interleaved address for one of a sequence of data values comprising: a logic circuit for determining whether an interleaved address is set for each of the sequence of data values, and, if not, the logic circuit providing a signal to increment each counter value by a substantially equivalent increment value, the increment value determined by the counter value generating the tentative address set as the interleaved address (col. 7, lines 11-12, lines 35-43, Pekarich et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ikeda et al.'s patent with the teachings of Pekarich et al. by including an additional step of using the interleave address generator comprising logic circuits.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the interleave address generator comprising logic circuits would provide the opportunity to determine whether an interleaved address is set for each data sequence and provide a signal to generate the interleaved address.

- As per claim 14, Ikeda et al. and Pekarich et al. teach the additional limitations.

Ikeda et al. teach a turbo encoder, wherein said interleave address generator comprises: an output symbol number generator for sequentially generating symbol numbers for an interleaver input sequence stored in said interleaver memory (figure 7, 9, page 7, paragraph 221, page 8, paragraph 230, Ikeda et

al.); and a threshold selector for setting a unique threshold for each of the symbol numbers generated by said output symbol number generator (page 6, paragraph 166, page 8, paragraph 229, 231, Ikeda et al.).

- As per claim 15, Ikeda et al. and Pekarich et al. teach the additional limitations.

Ikeda et al. teach a turbo encoder, wherein: said threshold selector selects a plurality of thresholds in accordance with the number of information bits of said interleaver input sequence, wherein said thresholds each correspond to an output symbol number generated by said output symbol number generator for each of the number of information bits of said interleaver input sequence, said output symbol number generator possibly generating an address, the value of which exceeds the number of bits excluding tail bits from the number of information bits of said interleaver input sequence (table 2, page 3, paragraph 69-74, page 6, paragraph 166, Ikeda et al.).

- As per claim 16, Ikeda et al. and Pekarich et al. teach the additional limitations.

Ikeda et al. teach a turbo encoder, wherein: said interleave address generator comprises an offset selector for selecting an offset, said offset being added to the output symbol number from said output symbol number generator, in accordance with a threshold value selected from said threshold selector (page 6, paragraph 166, page 8, paragraph 229, 231, Ikeda et al.).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

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